of that required for most high reliability applications and the devices have already undergone successful qualification for space flight use [9]. These predictions of excellent reliability of the GaAs MESFET are reinforced by long-running device life tests at room temperature where 11 devices have so far accumulated $\frac{1}{2}$ million device hours with no device failures, a failure being defined as a parameter change greater than 10 percent.

ACKNOWLEDGMENT

The authors wish to thank their colleagues at the Allen Clark Research Center of The Plessey Company for their contributions.

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Reliability Study of GaAs MESFET's

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***Abstract*—Failure modes have been studied phenomenologically on a small-signal GaAs MESFET with a 1-μm aluminum gate. Three major failure modes have been revealed, i.e., gradual degradation due to source and drain contact degradation, catastrophic damage due to surge pulse, and instability or reversible drift of electrical characteristics during operation. To confirm the product quality and to assure the device reliability, a quality assurance program has been designed and incorporated in a production line. A cost-effective lifetime prediction method is presented that utilizes correlations between RF parameters and dc parameters calculated using an equivalent circuit model. Mean time to failure (MTTF) value of over 10^8 h has been obtained for the GaAs MESFET for an operating channel temperature of 100°C.**

I. INTRODUCTION

BECAUSE of its inherent superiority in high-frequency and low-noise capabilities, the GaAs MESFET is now establishing a firm position in the family of microwave semiconductor devices. Recent progress in device design and in manufacturing technology has demonstrated that commercial production of small-signal GaAs MESFET's is feasible, and the device is now being used in practical low-noise amplifiers for *C*- to *X*-band frequencies.

In order for the GaAs FET's to be used extensively and reliably in many applications, it is necessary to establish a reliability assurance system, which should be based on a cost-effective means of life prediction. Such a reliability assurance system is particularly important in space applications and in some sort of communication systems, where an extremely high degree of reliability is required.

The purpose of this paper is to present the results of our investigations of the following three problems: 1) What kinds of failure modes exist that govern the reliability of the GaAs MESFET? 2) How and what quality assurance program is to be designed to manufacture high reliability GaAs MESFET's? 3) How can the operational lifetime or reliability be evaluated or predicted with cost-effective techniques?

The investigations have been made on a GaAs MESFET with

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a 1-μm-length aluminum Schottky barrier gate. Tests in the laboratory and field have shown that the observed defective behavior in the GaAs MESFET can be classified into three categories:

1) gradual degradation, mainly due to ohmic contact degradation;
2) catastrophic damage due to surge pulses;
3) time-dependent instability or relatively slow reversible drift of electrical characteristics, probably related to the quality of the GaAs crystal.

Among the three failure modes, type 2) can be prevented to some extent by proper circuit design, and type 3) can be eliminated through initial testing and more effectively by proper selection of GaAs epitaxial wafers. Consequently, the failure mode of type 1), or gradual degradation, is considered to be the major factor in determining the lifetime of the device.

Referring to these results, we have designed a qualification assurance program for production of high reliability GaAs MESFET's. The program includes various inspections and tests, screening processes, and qualification tests for high reliability assurance. The practical usefulness of this program has been confirmed in the production of the GaAs MESFET.

In the reliability assurance system a cost-effective means for reliability or lifetime prediction is necessary. For this purpose a small-signal equivalent circuit model has been utilized to predict the variations of RF parameters, such as noise figure and power gain, versus the variations of device parameters such as transconductance. By utilizing such correlations and by combining the acceleration life test concept, reliability or lifetime can be predicted with a relatively simple life test.

Some details of the GaAs MESFET are described in Section II, failure modes and some related considerations are described in Section III, and a quality assurance program is described in Section IV with the aid of a flow diagram. In Section V the method of reliability or lifetime prediction is presented.

II. GaAs MESFET

The device under consideration is a GaAs MESFET with an aluminum Schottky barrier gate 1 μm long and 300 μm wide. Fig. 1 shows a top view of the GaAs FET element. The gate is a V patterned stripe of a 0.6-μm-thick vacuum-evaporated aluminum film, while the source and drain electrodes are evaporated and alloyed Au-Ge/Pt films of 0.19-μm thickness. This ohmic contact was prepared by vacuum evaporation of 88 percent Au–12 percent Ge alloy to 0.15-μm thickness and successive deposition of Pt with 0.04-μm thickness, and then alloying at 500°C for 30 s in a hydrogen atmosphere [1]. The source, drain, and gate electrodes are prepared on the surface of a rectangular mesa of an n-type epitaxial layer (doping density $N \simeq 1.5 \times 10^{17}$ cm^{-3}, thickness $\simeq 0.2$ μm). A buffer layer with apparent doping density of 10^{13}–10^{14} cm^{-3}, several microns thick, has been introduced between the active layer and the semiinsulating substrate. The buffer layer and the active n-type layer are grown continuously in a Ga/$AsCl_3$/H_2 vapor epitaxial process. The semiinsulating substrate is Cr-doped GaAs with a specific resistivity of about 10^8 $\Omega \cdot$ cm. The gate pad for lead wire bonding is on the buffer layer outside the mesa, and consists of a Ti/Pt/Au film, 0.7 μm thick, which prevents undesirable alloy formation between the gold wire and the gate aluminum. The bonding pads of the same Ti/Pt/Au film are provided on the source and drain contacts. No dielectric film passivation has been applied to the surface of the GaAs element. The semiconductor element is sealed hermetically in a stripline-type ceramic package with small parasitic capacitance (refer to Fig. 2). Typical electrical characteristics of the GaAs MESFET are listed in Table I.

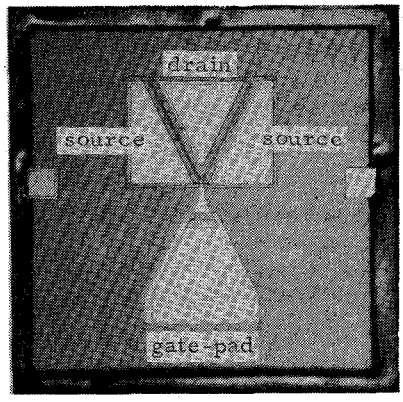


Fig. 1. Top view of the GaAs MESFET element.

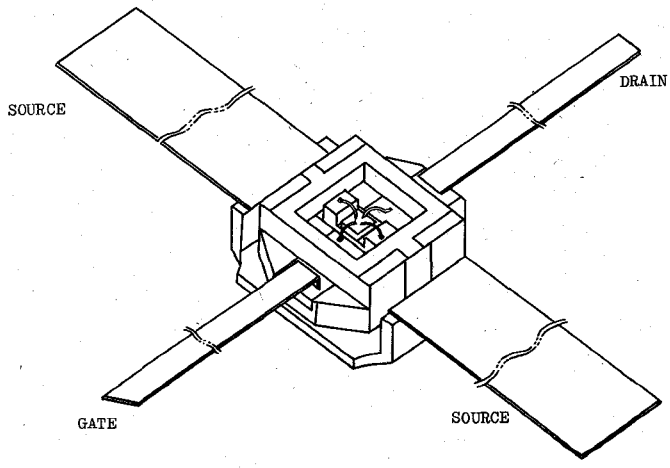


Fig. 2. Stripline-type ceramic package.

III. Failure Modes

Adequate understanding of failure modes is very important for the design of a quality assurance program and reliability evaluation system.

In order to find and analyze the probable defective behavior which may appear when the unscreened GaAs MESFET's are subjected to either long-term or short-term operation, we have conducted acceleration life tests, surge

TABLE I
TYPICAL CHARACTERISTICS OF GaAs FET

PARAMETER	SYMBOL	TEST CONDITION	VALUE
GATE PINCH-OFF VOLTAGE	V_P	V_D= 3V I_D= 0.1mA	3V
TRANSCONDUCTANCE	g_m	V_D= 3V, I_D= 30mA	20mmho
DRAIN CURRENT	I_{DSS}	V_D= 3V, V_G= 0V	60mA
GATE BREAKDOWN VOLTAGE	BV_{GS}	I_G = 10μA	15V
NOISE FIGURE	NF	V_D = 3V, I_D = 10mA f = 8GHz	3.5dB
MAXIMUM AVAILABLE GAIN	MAG	V_D= 3V, I_D= 30mA f = 8GHz	10dB
MAXIMUM FREQ. OF OSCILLATION	f_{max}	V_D= 3V, I_D = 30mA	60GHz

Note: V_D: drain voltage. I_D: drain current. V_G: gate voltage. I_G: gate current. f: frequency.

TABLE II
LIFE-TEST CONDITIONS

TEST	TEST CONDITION	SAMPLE SIZE
HIGH TEMPERATURE STORAGE	T_a = 227°C	20
	T_a = 259°C	20
	T_a = 295°C	20
GATE BIASING AT HIGH TEMPERATURE	V_G = - 5 V T_a = 150°C	20
OPERATION LIFE TEST	P_D = 120 mW T_a = 25°C	18
	P_D = 240 mW T_a = 25°C	18

Note: T_a: ambient temperature. V_G: gate voltage. P_D: power dissipation.

TABLE III
DEVICE PARAMETERS MONITORED IN THE LIFE TESTS AND THEIR MAXIMUM ALLOWANCE FOR DEGRADATION OR DRIFTS

PARAMETER	SYMBOL	CONDITION	MAX. ALLOWANCE*
DRAIN CURRENT	I_{DSS}	V_D = 3V, V_G= 0V	± 10%
SPECIFIC DRAIN CURRENT	I_{DS}	V_D=0.5V, V_G=0V	± 25%
PINCH-OFF VOLTAGE	V_P	V_D=3V, I_D= 0V	± 10%
TRANSCONDUCTANCE	g_m	V_D= 3V, I_D= 30mA	± 10%
GATE FORWARD VOLTAGE	V_{GF}	I_{GF} = 20mA	± 20%
GATE REVERSE CURRENT	I_{GS}	V_G = -5V, V_D= 0V	10 times initial value or 1μA whichever is greater

* Equivalent to failure criterion. I_{GF}: gate forward current.

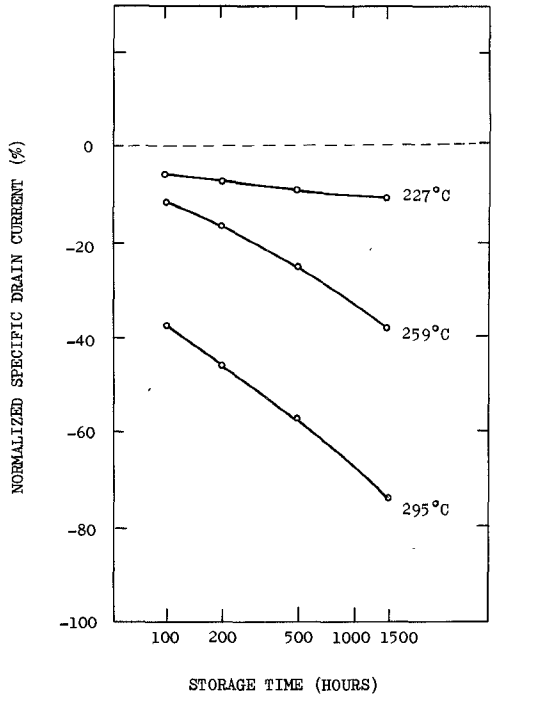


Fig. 3. Variation of the specific drain current I_{DS} (at V_D = 0.5 V) observed in high-termperature storage at three different stress levels. The variation is normalized with respect to the initial value.

tests, and relatively short-term instability tests. In this section results of these tests together with some brief considerations of failure mechanisms are described.

A. Life-Test Results

Several life tests were carried out which include 1) high temperature storage at 227, 259, and 295°C for 1500 h, 2) gate reverse biasing at 150°C ambient for 500 h, and 3) power burn-in with 120 and 240-mW power dissipation for 500 h. Test conditions are listed in Table II. In these tests the device parameters listed in Table III were monitored.

Throughout all these tests significant variation in parameter values was observed only in the specific drain current I_{DS} (drain current in the unsaturated region; V_D = 0.5 V) in the high-temperature storage tests. Fig. 3 shows a gradual decrease of I_{DS} with aging time, observed in the high-temperature storage. In the power burn-in tests I_{DS} did not show such marked variation, probably because of the lower temperatures in the power burn-in tests. As for the other parameters, variations are all within ±10 percent in every test, except the change of gate reverse current I_{GS}, which varied within ±50 percent range or more, but did not exhibit any tendency of degradation.

As shown in Fig. 3, the decrease of I_{DS} is more pronounced

with higher temperature. It should be noted that I_{DS} is the drain current in the voltage region, where the current does not saturate, versus drain-source voltage V_D. Therefore the decrease of I_{DS} is equivalent to an increase of the resistance between source and drain. Since the gate pinch-off voltage V_p showed no change in the tests, any change in physical parameters of the active epitaxial layer is not likely, and the decrease of I_{DS} is considered to be due to an increase in the source and drain contact resistances. From the temperature dependence of this degradation mode, the activation energy for the degradation process was estimated to be about 1.8 eV.

It has been shown by Ohata and Ogawa [1] that the Au-Ge/Pt ohmic contact forms a two-layer structure of Au-Ga/Pt-As-Ge on GaAs, which is fairly stable when subjected to thermal aging. The initial specific contact resistance of this ohmic contact is estimated to be as low as $10^{-6}\ \Omega \cdot \mathrm{cm}^2$. A probable physical mechanism of the long-term gradual degradation of the Au-Ge/Pt contact might be a very slight penetration of the alloy front into the n-type active layer increasing the sheet resistance of the n-type layer beneath the contact and/or a very slow formation of a high resistance layer beneath the contact due to gradual generation of point defects and/or dislocations in the immediate vicinity of the contact.

The results of the aforementioned life tests have led to a conclusion that the major failure mode that governs the device life due to long-term degradation is the ohmic contact degradation in the source and drain electrodes.

B. Surge-Test Results

It is common to have a semiconductor device fail during surge pulse application. Therefore durability against surge pulse can be a useful measure of the ruggedness of the device.

Fig. 4 shows results of the surge tests where a rectangular pulse was applied between the gate and the source (upper curve; negative pulse was applied) and between the drain and the source (lower curve; positive pulse was applied). The ordinate of the figure indicates the critical voltage for burnout damage. As seen in the figure, surge application to the gate in reverse direction does not damage the device up to over 40 V. On the other hand, a surge pulse to the drain degrades the device even at relatively low voltage amplitudes. Most of the damaged device elements in those tests showed the appearance illustrated in Fig. 5, where localized burnout is observed between the electrodes. In some damaged devices, however, no visible change in appearance was observed. In such devices permanent breakdown in the GaAs crystal, or some anomalous switching phenomenon as observed by Rossel *et al.* [2], might occur.

The ruggedness of the device against such surge pulses would be enhanced by improving the uniformity (elimination of irregularity) of the electrode edges through refinements in fabrication technology. Also, the device failure due to surge pulses can be avoided to some extent by properly designing the circuit in which the device is incorporated.

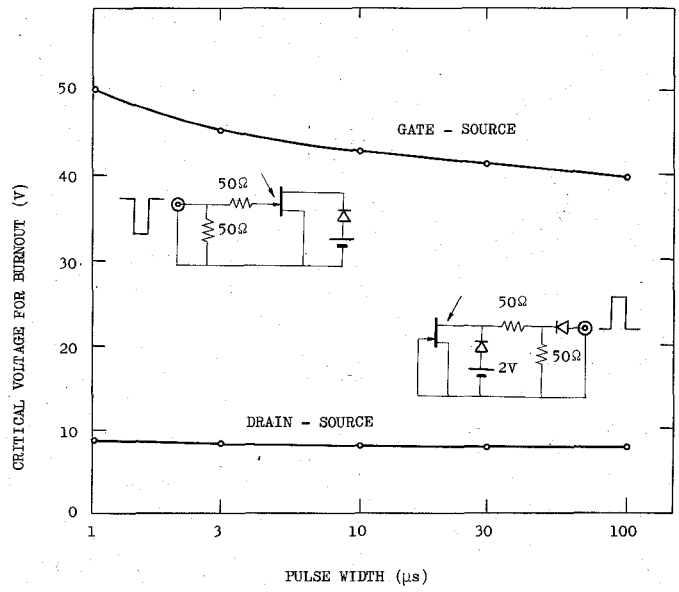
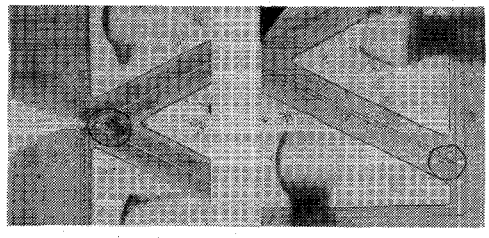


Fig. 4. Surge-test results. The voltages are measured at points indicated by an arrow.



(a) (b)

Fig. 5. Photographs of the GaAs MESFET elements damaged by surge pulses applied (a) between drain and source, and (b) between gate and source.

C. Instability or Drift of RF Parameters

In some devices drift phenomena of RF parameters were observed when the device was turned on to operating bias condition. This drift, usually associated with drift of some dc parameters, is reversible; and the device parameters return to their original values after some time if the device is turned off. In Fig. 6 an example of such a drift phenomenon is shown, where the noise figure NF, associated gain G_A (both measured at 4 GHz), and drain current I_D are plotted versus the elapsed time after turn on. Each parameter drifts in a time scale of minutes. The time required for the full recovery after turn off is almost of the same order as that of the turn-on drift. The time scale differs among samples and ranges from seconds to hours. Obviously, the presence of the drift phenomenon as previously described is undesirable in device applications.

The devices that exhibit the drift phenomenon usually come from specific epitaxial wafers, or in other words, the drift phenomenon appears in some particular wafer lots.

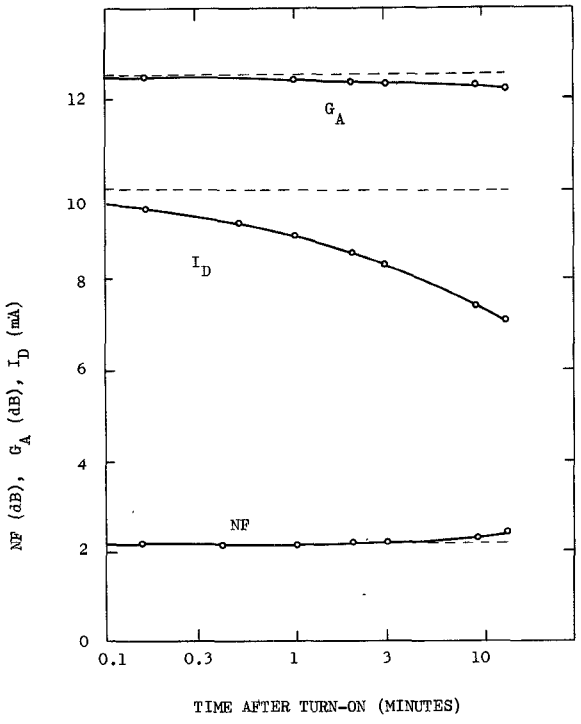


Fig. 6. Drifts of noise figure (NF), associated gain (G_A), and drain current I_D, after the dc bias is switched on (V_D = 3 V).

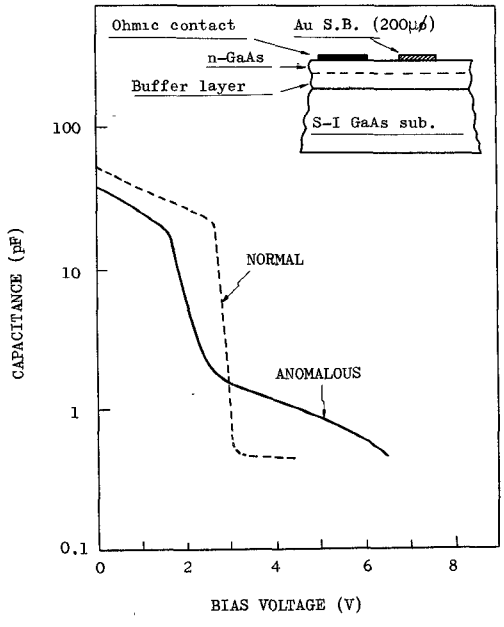


Fig. 7. Capacitance-voltage relationship of a Schottky barrier formed on the epitaxial layer.

In general, the wafer from which the drifting devices are produced, exhibits a somewhat anomalous behavior in the capacitance-voltage dependence of a Schottky barrier formed on the epitaxial layer surface (see inset in Fig. 7) for doping profile measurement. In Fig. 7 the capacitance versus reverse bias voltage obtained from a good epitaxial wafer (showing no drift) and from a wafer exhibiting the drift phenomenon are shown. The anomalous capacitance-voltage dependence as shown in Fig. 7 suggests that a considerable amount of deep-level carrier-trapping centers may exist in the vicinity of the interface between the active layer or the buffer layer and the semiinsulating substrate. At the present stage of the investigation, we are not completely certain that the drift phenomenon is exclusively related to the capacitance-voltage dependence. However, what we can say at this time is that at least most of the defective epitaxial wafers can be rejected if the capacitance-voltage relationship is carefully analyzed.

TABLE IV
FAILURE MODES OF GaAs MESFET

Failure Mode	Phenomenon	Physical Cause
(a) Long-term gradual degradation	Gradual decrease of I_{DS}	Increase of ohmic contact resistance
(b) Damage due to surge pulse	Burn out	Localized electric field concentration due to irregularity
(c) Instability or reversible drift	Reversible drift of NF, MAG etc. Reversible decrease of I_D	Epitaxial-layer substrate interface problems (due to deep traps) ? Other unknown effect ?

D. Life-Limiting Failure Mode

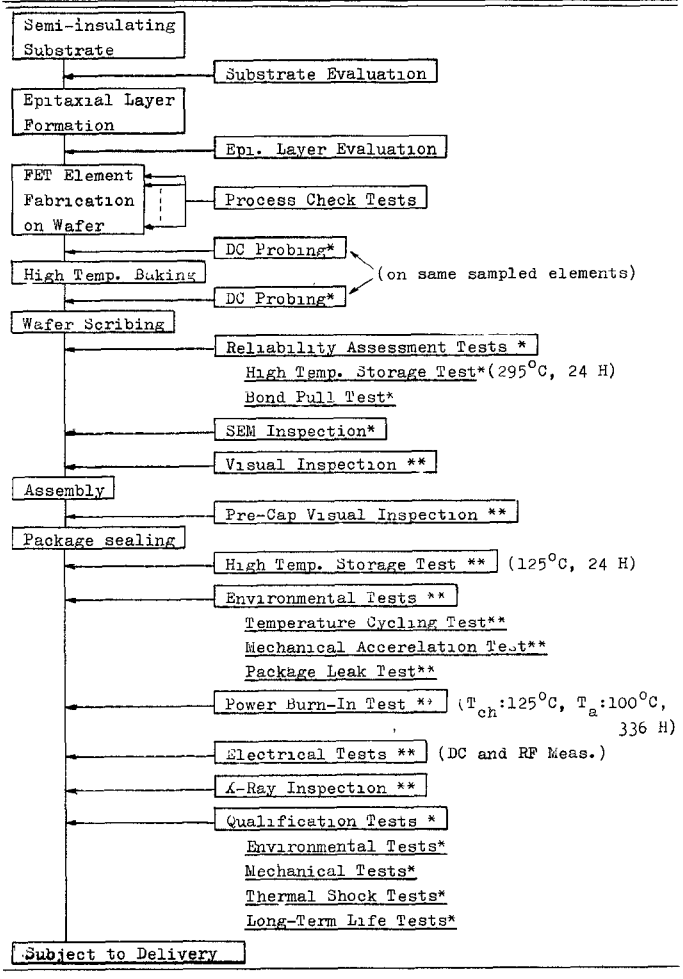
As described in Sections III-A–III-C, failure modes observed in the GaAs MESFET can be classified into three major categories, i.e., 1) long-term gradual degradation, mainly due to contact resistance degradation, 2) catastrophic damage due to a surge pulse, and 3) instability or reversible drift of electrical characteristics. These are summarized in Table IV. Of the three categories, 3) is an initial defect rather than a failure. Of course, the aforementioned failure modes are those observed in the present study, and there might be other types of failures or other physical origins. Of the three failure modes, type 2) can be prevented by a proper circuit design and also by careful processing and refinement of fabrication processes. Type 3) mode can be preventively rejected by proper selection of epitaxial wafers and by initial testing.

Therefore type 1) mode is the major life-limiting failure mode, as described in Section III-A.

IV. QUALITY ASSURANCE PROGRAM

In order to produce the devices that meet the design criteria and are free from failure potential, the manufacturing processes must be well controlled and monitored, and the reliability of produced devices must be confirmed. The essential philosophy of a program for such purposes must be 1) to confirm whether individual manufacturing processes, materials, components, and other factors affecting the product quality are as specified, 2) to select only the well-processed devices and reject the ones having any

TABLE V
QUALITY ASSURANCE PROGRAM FOR HIGH RELIABILITY GaAs FET



* Sampling basis.
** 100 percent testing.

failure potential, and 3) to confirm or evaluate the reliability of the produced devices.

In Table V a flow diagram is shown, which demonstrates how the quality assurance program is incorporated in the manufacturing processes of the GaAs MESFET's for high reliability applications. The program includes various inspections, tests, and measurements. In the following, a brief explanation of the quality assurance program in Table V is given.

A. Quality Control Inspections

Quality control (QC) inspections are incorporated at each key step in the manufacturing process. The purpose of the inspections is of course to check whether the relevant procedures, materials, etc., meet the proper standards.

Inspections on the semiinsulating substrate and on the epitaxial layers are important not only for obtaining good electrical performance but also for preventive rejection of the instability or drifts as described in Section III-C. For the evaluation of the substrate material, measurements of high field breakdown characteristics are adopted in addition to the inspection of etch pit density and of specific resistivity. As for the evaluation of the epitaxial layers including both the active layer and the buffer layer, a measurement of the capacitance-voltage relationship mentioned in Section III-C is the most important inspection. This measurement gives information on doping density, thickness of the active layer, gate pinch-off voltage, and some prediction about the drift characteristics.

Several process check tests are made during FET element fabrication on the GaAs wafer. The tests include checking of metallizations and some dc probe tests. After the FET element fabrication is finished, a high-temperature baking (for example, 200°C for 48 h) is carried out. Before and after the baking, dc probing of several sampled elements is made, and changes of electrical characteristics due to the baking are checked on each sampled element.

B. Reliability Assessment Tests

After the wafer scribing, several chips per wafer are sampled, and subjected to reliability assessment tests. The tests consist of 1) high-temperature storage (acceleration test) at a relatively high stress level (295°C, 24 h) in nitrogen, and 2) bond pull tests, which check the adhesive strength of the bonding wire. As will be discussed in Section V, the condition of the high-temperature stress level has been determined on the basis of the failure analysis on gradual degradation. If the sampled units do not degrade with respect to some specified criteria, then the sampled batch is expected to have potentially the reliability or mean time to failure (MTTF) of several times 10^8 h (refer to Section V). By this test the reliability of the batch can be assessed rather simply in a relatively short time.

C. Screening

Before the GaAs MESFET chips are assembled in the package, inspections with the scanning electron microscope (SEM) and by visual observation are made. These are in some sense QC inspections. However, the purpose of the inspections is to select only the well-processed chips and reject the defective ones. After the assembly all specimens are subjected to precap visual inspection. After the package sealing several screening processes are carried out on a 100 percent basis. They range from a high-temperature storage test at 125°C for 24 h, to X-ray inspection. In environmental tests all products are subjected to a temperature cycling test, mechanical acceleration test, and package leak test. In the high-temperature storage test, in each environmental test, and in the power burn-in test, major electrical characteristics are measured and documented, and data before and after each test are compared. If the deviation of the parameter exceeds the maximum specified allowance, the specimen is rejected.

In electrical measurement tests a check test for the drift phenomenon is made based on a specified criterion.

Through X-ray inspection, any failure potential due to an incorrect configuration of the bonding wire and so on, can be detected.

D. Qualification Tests

The purpose of the qualification tests is to certify the reliability of a manufacturing batch (wafer lot) through destructive tests on specimens sampled from the relevant batch. The qualification tests are applied to devices which require reliability certification, or to devices that require extremely high reliability such as for space applications. The qualification tests consist of 1) environmental tests, 2) mechanical shock tests, 3) thermal shock tests, and 4) long-term life tests (usually requiring several months).

In a quality assurance program various criteria for judging whether the specimen is allowed to go to the next step are specified by considering the reliability required; and therefore the criteria are not, in principle, rigidly specified.

The quality assurance program has been incorporated in a production line, and has made a useful contribution to the production of high reliability GaAs MESFET's.

V. Reliability or Life Prediction

A cost-effective way of reliability or lifetime prediction is an important problem in quality assurance. Our methodology of establishing the prediction system is based on the following procedures: 1) to specify the failure criteria, or to specify allowable degrees of degradation or drifts, in terms of allowable deviation of specific RF parameters; 2) to find the correlations between the RF parameter variation and dc parameter variation; 3) to calculate the allowable range of dc parameter deviation; 4) to find the activation energy or temperature dependence of the dc parameter degradation in long-term operation; 5) to utilize the temperature dependence of the degradation and acceleration life-test results for the reliability or lifetime prediction.

We have tentatively set the allowable RF parameter deviation at 0.5-dB NF variation and 2-dB MAG variation, each from the initial value, at 4 GHz. These criteria have come from requirements in various field applications. Of course, these criteria should be changed depending on the reliability required.

To find the correlations between the RF parameters and dc parameters, a computer calculation has been made using an equivalent circuit as shown in Fig. 8. By incorporating a parasitic resistance increase that corresponds to the ohmic contact degradation described in Section III-A, the allowable maximum drift range of the specific drain current I_{DS}, low-frequency transconductance g_m, and gate forward voltage V_{GF} was estimated. By considering the calculated results, the maximum allowable range of other parameters was also specified. The resultant allowable deviations are listed in Table III.

The device life or MTTF has been estimated based on the assumption that the major failure mode in long-term operation is the contact resistance degradation (refer to Section III-D). A failure criterion has been defined as 25 percent decrease of the specific drain current I_{DS}. MTTF versus reciprocal absolute temperature ($1/T$) lines were drawn for 20 percent decrease and 30 percent decrease of I_{DS} as shown in Fig. 9, by using the high-temperature

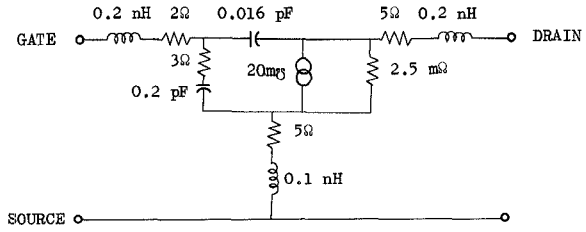


Fig. 8. Small-signal equivalent circuit of the GaAs MESFET.

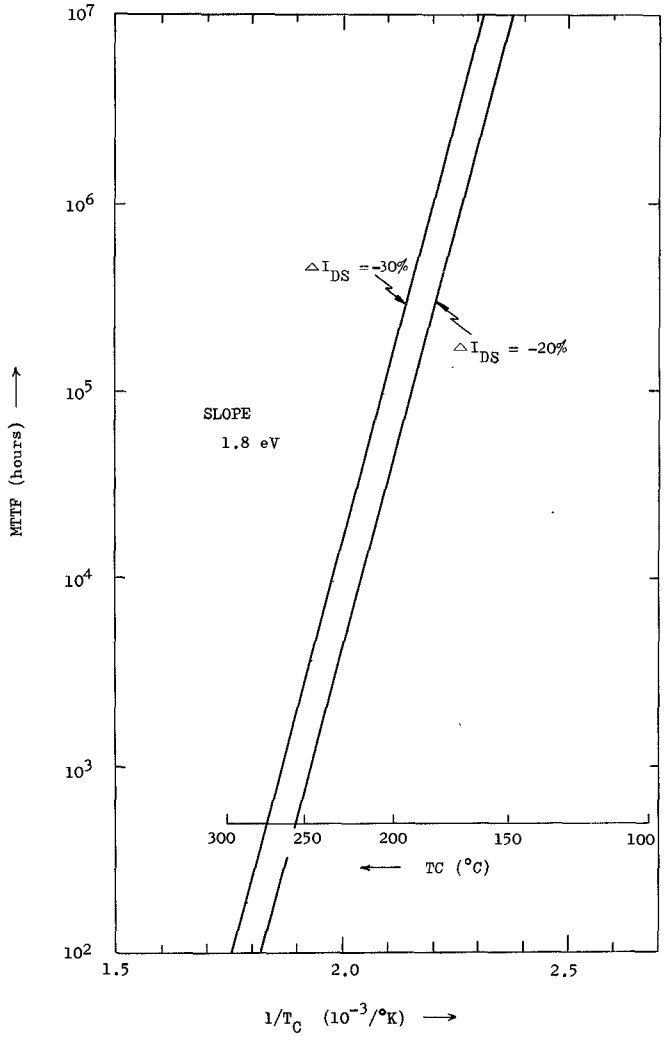


Fig. 9. MTTF versus reciprocal absolute temperature of the channel, obtained in high-temperature storage tests.

storage-test results described in Section III-A. The two lines are almost parallel and their activation energy has been determined to be approximately 1.8 eV. By extrapolation of these lines, an MTTF value of about 3×10^8 h has been obtained for an operating channel temperature of 100°C, using the preceding criterion.

A line corresponding to $\Delta I_{DS} = -25$ percent, which lies between the two lines, crosses the point for 295°C channel temperature and for 24 h MTTF. Therefore if in the reliability assessment tests (see Table V) more than a half of the sampled devices do not exhibit the failure specified by the

criterion, the relevant population batch is estimated to have a reliability corresponding to MTTF of 3×10^8 h at 100°C channel temperature. The reliability or lifetime prediction in such a way is relatively inexpensive and effective and requires only a relatively short time.

A more accurate prediction or certification of the reliability can be made with a long-term operation life test performed in the qualification tests (refer to Section IV-D).

VI. Conclusion

Although the GaAs MESFET has been recognized to be a very promising device for microwave applications, little has been known so far about device reliability [3], [4].

In this paper failure modes of the GaAs MESFET have been studied through experimental investigations on a 1-μm aluminum Schottky barrier gate GaAs FET for low-noise amplification. Three major modes have been observed, i.e., long-term gradual degradation due to ohmic contact degradation, catastrophic burnout due to a surge pulse, and instability or reversible drift of electrical characteristics during operation.

To confirm the product quality and to assure the device reliability, a quality assurance program has been designed and incorporated successfully in the production line. The program includes various QC inspections, reliability assessment tests, screening processes, and qualification tests for reliability certification.

A cost-effective means of reliability or lifetime prediction has been described which utilizes the results of the failure mode analyses and of the correlations between RF parameters and dc parameters. A simulation based on an equivalent circuit model has been utilized to derive the correlations.

A MTTF value of approximately 3×10^8 h has been obtained for the GaAs MESFET for 100°C channel temperature. Although this MTTF value is sufficiently high for most applications, it is still lower than that obtained in high-reliability silicon bipolar transistors for lower microwave frequencies, which attain a MTTF of 10^{10} h.

As has been described, the MTTF of the GaAs MESFET is mainly governed by the contact degradation. Improvement of the contact technology must be made which would increase the MTTF of the GaAs MESFET. When such an improvement has been made, there might be other failure modes not discussed in this paper. Surface passivation might be a necessary problem to be solved to achieve a high reliability comparable to that of silicon bipolar transistors for high reliability applications.

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